GUJARAT UNIVERISTY

B.E. Sem 8th EC

Digital System Design

Each question carry 10 marks

Q 1. Draw a timing diagram and illustrate your understanding of SET UP and HOLDING time. Give a qualitative description of each and how these specification relate to the hardware of the flip-flop.

Q.2 In your words discuss clock skew. Discuss why clock skew can create data transmission problems.

Q. 3 List types of sequential Machines. Give also difference between them.

Q. 4 Explain Moore and Mealy Machine with suitable example.

Q.6 Draw and explain Moore Machine for BCD counter.

Q.7 Draw and explain Mealy Machine for BCD counter.

Q. 8 Draw and explain architecture of FPGA.

Q.9 Draw and explain architecture of CPLD.

Q, 10 Explain difference between FPGA and CPLD.

Q.11 Draw and explain block diagram of two bit comparator with truth table. Simplified expression for the comparator using K'map and also draw gate level circuit for it.

Q.12 Draw and explain block diagram of 4 to 1 with truth table. Simplified expression for the comparator using K'map and also draw gate level circuit for it.

Q. 13 Explain with combinational design using decoder with suitable example.

Q. 14 Explain any two code converter circuit with necessary figures and truth tables.

Q. 15 Draw and explain implementation of priority encoder.

Q. 16 Draw and explain implementation of three element encoder.

Q. 17 Explain significance of wired logic. Also give practical aspects of wired logic and bus oriented structures.

Q.18 Implement the following functions using 4 to 16 decoder with low asserted outputs

a) $F1 (A,B,C,D) = \Sigma (0,1,4,7,9,12,14)$

b) $F2 (A,B,C,D) = \Sigma (0,1,2,3)$

Q.19 Implement the following functions using 4 to 16 decoder with low asserted outputs

a) F1 (A,B,C,D) = Σ (0,3,6,7,9,13,15)

b) F2 (A,B,C,D) = Σ (0,4,5,7)

Q.20 Implement the following functions using 4 to 16 decoder with low asserted outputs

a) F1 (A,B,C,D) = Σ (0,2,4,8,9,10,14)

b) F1 (A,B,C,D) = Σ (0,2,3)

Q. 21 Design a controlled 2's complement four bit adder/subtractor using one 74283, four EXOR gates and one inverter. Shoe that your circuit can be slightly modified to make a 1's complement adder/subtractor.

Q. 22 Explain synchronous analysis process with suitable example.

Q. 23 Write design steps for traditional synchronous sequential circuits.

Q. 24 Explain state reduction process with suitable example.

Q. 25 Draw and explain block diagram, state diagram and timing diagram of modulo 6 binary counter. Also draw its schematic diagram.

Q. 26 Draw and explain block diagram, state diagram and timing diagram of modulo 5 binary counter. Also draw its schematic diagram.

Q. 27 Draw and explain block diagram, state diagram and timing diagram of modulo 10 binary counter. Also draw its schematic diagram.

Q. 28 Design a three bit, modulo 6, unit distance code, up-down counter with a synchronous CLEAR.

Q. 29 Explain significance of multimode counter.

Q. 30 Explain use of MSI Decoders in system controllers with suitable example.

Q. 31 Explain use of MSI multiplexer in system controllers with suitable example.

Q. 32 Explain use of PROM in system controllers with suitable example.

Q. 33 Explain use of PLA in system controllers with suitable example.

Q. 34 Explain concept of Programmable system controller.

Q. 35 Explain concept of Asynchronous analysis with suitable example.

Q. 36 Explain design of Asynchronous machine with suitable example.

Q. 37 Explain cycle and races with suitable example.

Q. 38 Write short note

1) Hazards 2) Essential hazarads.

Q. 39 Design circuit for sequence detector using mealy Machine for following sequence

1) 11001 2) 11011

Q. 40 Design circuit for sequence detector using Moore Machine for following sequence

1) 11001 2) 11011

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